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Search Results -

Terms	Documents
L2 and arbit$5	143

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L3

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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	L2 and arbit$5	143	L3
L2	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	187	L2
DB=DWPI; PLUR=YES; OP=OR			
L1	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	2	L1

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Search Results -

Terms	Documents
L3	0

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L4

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Search History

DATE: Thursday, September 12, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	L2 and arbit$5	143	L3
L2	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	187	L2
DB=DWPI; PLUR=YES; OP=OR			
L1	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	2	L1

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Search Results -

Terms	Documents
L1 and arbit?	0

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1 and arbit$5?

Refine Search

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Search History

DATE: Thursday, September 12, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L2	L1 and arbit?	0	L2
L1	(transaction or task or job) same (queue or FIFO) same grant same bus	115	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
l6 and ((deadlock or livelock) same retr$3)	33

Database:
- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L7

Refine Search

Recall Text | Clear

Search History

DATE: Thursday, September 12, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L7	l6 and ((deadlock or livelock) same retr$3)	33	L7
L6	(deadlock or livelock) same bus same (bridge or expansion)	112	L6
L5	(deadlock or livelock) same (split adj1 bus) same (bridge or expansion)	5	L5
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	L2 and arbit$5	143	L3
L2	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	187	L2
DB=DWPI; PLUR=YES; OP=OR			
L1	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	2	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L7	0

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L8

Refine Search

Recall Text | Clear

Search History

DATE: Thursday, September 12, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L8	L7	0	L8
DB=USPT; PLUR=YES; OP=OR			
L7	l6 and ((deadlock or livelock) same retr$3)	33	L7
L6	(deadlock or livelock) same bus same (bridge or expansion)	112	L6
L5	(deadlock or livelock) same (split adj1 bus) same (bridge or expansion)	5	L5
DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	L2 and arbit$5	143	L3
L2	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	187	L2
DB=DWPI; PLUR=YES; OP=OR			
L1	(transaction or task or job) same (queue or FIFO) same grant$3 same bus	2	L1

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Search Results -

Terms	Documents
(710/311)!.CCLS. or 710/110.ccls. or 710/107.ccls. or 710/263.ccls. or 710/41.ccls. or 710/41.ccls. or 710/52.ccls. or 709/100.ccls. or 709/208.ccls. or 714/47.ccls. or 711/151.ccls.	3587

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear

Search History

DATE: Thursday, September 12, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L1	(710/311)!.CCLS. or 710/110.ccls. or 710/107.ccls. or 710/263.ccls. or 710/41.ccls. or 710/41.ccls. or 710/52.ccls. or 709/100.ccls. or 709/208.ccls. or 714/47.ccls. or 711/151.ccls.	3587	L1

END OF SEARCH HISTORY

WEST

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Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
L3 and (deadlock or livelock)	52

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear

Search History

DATE: Thursday, September 12, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	L3 and (deadlock or livelock)	52	L4
L3	l1 and L2	218	L3
L2	(transaction or task or job) same grant$3 same bus	980	L2
L1	(710/311)!.CCLS. or 710/110.ccls. or 710/107.ccls. or 710/263.ccls. or 710/41.ccls. or 710/41.ccls. or 710/52.ccls. or 709/100.ccls. or 709/208.ccls. or 714/47.ccls. or 711/151.ccls.	3587	L1

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Then click **Search Again**.

((transaction or task or job))and ((arbit* and grant*))

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

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1 **Point-to-point connectivity between neuromorphic chips using add events**
Boahen, K.A.
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transact
Volume: 47 Issue: 5 , May 2000
Page(s): 416 -434

[Abstract] [PDF Full-Text (888 KB)] **JNL**

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2 **Evolving rules for a self-organizing finite element mesh generation algorithm**
Langham, A.E.; Grant, P.W.
Evolutionary Computation, 1999. CEC 99. Proceedings of the 1999 Congress
-168 Vol. 1

[Abstract] [PDF Full-Text (1052 KB)] **CNF**

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3 **Performance enhancement through joint detection of cochannel si using diversity arrays**
Grant, S.J.; Cavers, J.K.
Communications, IEEE Transactions on , Volume: 46 Issue: 8 , Aug. 1998
Page(s): 1038 -1049

[Abstract] [PDF Full-Text (340 KB)] **JNL**

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4 **Performance model for a prioritized multiple-bus multiprocessor s**
John, L.K.; Yu-Cheng Liu
Computers, IEEE Transactions on , Volume: 45 Issue: 5 , May 1996

Page(s): 580 -588

[Abstract] [PDF Full-Text (724 KB)] **JNL**

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5 **CMOS design of the tree arbiter element**
Josephs, M.B.; Yantchev, J.T.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume 4 , Dec. 1996
Page(s): 472 -476

[Abstract] [PDF Full-Text (392 KB)] **JNL**

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6 **Some solutions for FIP network interconnection**
Saba, G.; Mammeri, Z.; Thomesse, J.P.
Factory Communication Systems, 1995. WFCS '95, Proceedings., 1995 IEEE International Workshop on , 1995
Page(s): 13 -20

[Abstract] [PDF Full-Text (620 KB)] **CNF**

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7 **A low latency asynchronous arbitration circuit**
Yakovlev, A.; Petrov, A.; Lavagno, L.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume 3 , Sept. 1994
Page(s): 372 -377

[Abstract] [PDF Full-Text (584 KB)] **JNL**

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8 **Orthogonal least squares learning algorithm for radial basis functi networks**
Chen, S.; Cowan, C.F.N.; Grant, P.M.
Neural Networks, IEEE Transactions on , Volume: 2 Issue: 2 , March 1991
Page(s): 302 -309

[Abstract] [PDF Full-Text (580 KB)] **JNL**

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9 **A finite-element method for the prediction of joule heating of cond electromagnetic launchers**
Auton, J.R.; Grant, C.R.; Houghton, R.L.; Thompson, H.P.
Magnetics, IEEE Transactions on , Volume: 25 Issue: 1 , Jan. 1989
Page(s): 63 -67

[Abstract] [PDF Full-Text (272 KB)] **JNL**

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SEARCH RESULTS [PDF Full-Text (724 KB)] PREVIOUS NEXT DOWNLOAD CITA

Performance model for a prioritized multiple-bus multiprocessor system

- John, L.K. Yu-Cheng Liu
Dept. of Comput. Sci. & Eng., Univ. of South Florida, Tampa, FL, USA

This paper appears in: Computers, IEEE Transactions on
On page(s): 580 - 588
May 1996
Volume: 45 Issue: 5
ISSN: 0018-9340
References Cited: 24
CODEN: ITCOB4
INSPEC Accession Number: 5294010

Abstract:
The performance of a shared memory multiprocessor system with a multiple-l interconnection network is studied in this paper. The effect of bus and memor contention is modeled using a probabilistic model and a closed form solution f acceptance probability of each processor is presented. It is assumed that eacl in the system has a distinct priority assigned to it and that arbitration is base priority. Whenever a request from a processor is rejected due to bus or memo conflicts, the request is resubmitted until granted. Based on the model, indivi processor acceptance probabilities are first estimated, from which the effectiv bandwidth is computed. The accuracy of the analytical model is verified basec simulation results. Results from the model are compared against other appro> models previously reported in literature. It is observed that the inaccuracy of measured in terms of error from simulation results is less than that in previou reported studies.

Index Terms:
shared memory systems performance evaluation multiprocessing systems sha memory multiprocessor system performance multiple-bus interconnection net prioritized multiple-bus multiprocessor acceptance probability distinct priority acceptance probabilities memory bandwidth

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SEARCH RESULTS [PDF Full-Text (392 KB)] PREVIOUS NEXT DOWNLOAD CITA

CMOS design of the tree arbiter element

- Josephs, M.B. Yantchev, J.T.
Centre for Concurrent Syst. & VLSI, South Bank Univ., London, UK

This paper appears in: Very Large Scale Integration (VLSI) Systems, IEEE Tra on
On page(s): 472 - 476
Dec. 1996
Volume: 4 Issue: 4
ISSN: 1063-8210
References Cited: 14
CODEN: IEVSE9
INSPEC Accession Number: 5442088

Abstract:
An asynchronous arbiter dynamically allocates a resource in response to requ processes. Glitch-free operation when two requests arrive concurrently is poss MOS technologies. Multiway arbitration using a request-grant-release-acknow protocol can be achieved by connecting together two-way arbiters (mutual ex tree arbiter elements). We have devised a fast and compact design for the tre element which offers eager forward-propagation of requests. It compares favc a well-known design in which request propagation must wait for arbitration to Our analysis and simulations also suggest that no performance improvement obtained by incorporating eager acknowledgment of releases. All of the desigr considered in this paper are speed-independent, a formal property of a netwo elements which can be taken as a positive indication of their robustness.

Index Terms:
CMOS logic circuits logic design resource allocation asynchronous circuits flip- integrated circuit design CMOS design tree arbiter element asynchronous arbi dynamical resource allocation glitch-free operation multiway arbitration request-grant-release-acknowledge protocol two-way arbiters

Documents that cite this document
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Reference list:

1. E. Brunvand, "Translating concurrent communicating programs into asynch circuits", *School Comput. Sci., Carnegie Mellon Univ.*, 1991.

2. T. J. Chaney, C. E. Molnar, "Anomalous behavior of synchroniser and arbite *IEEE Trans. Comput.*, vol.C-22, pp.421-422, Apr. 1973.

3. D. L. Dill, E. M. Clarke, "Automatic verification of asynchronous circuits usir logic", *Proc. IEE*, vol.133, no.5, pt.E, 1986.

4. D. L. Dill, "Trace Theory for Automatic Hierarchical Verification of Speed-In Circuits", *The M.I.T. Press*, Cambridge, MA, 1989.

5. J. Genrich, R. M. Shapiro, "Formal verification of an arbiter cascade", *Proc. Conf. Application Theory Petri Nets*, 1992.

6. A. J. Martin, "On Seitz' arbiter", *Comput. Sci. Dep., California Inst. Technol*

7. A. J. Martin, "Programming in VLSI: From communicating processes to delay-insensitive circuits", *Developments in Concurrency and Communication*, *Addison-Wesley*, Reading, MA, pp.1-64, 1989.

8. R. C. Pearce, J. A. Field, W. D. Little, "Asynchronous arbiter module", *IEEE Comput.*, vol.C-24, pp.931-932, Sept. 1975.

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10. C. L. Seitz, "Ideas about arbiters", *Lambda*, vol.1, pp.10-14, 1980.

11. C. L. Seitz, "System timing", *Introduction to VLSI Systems*, *Addison-Wesl* Reading, MA, pp.218-262, 1980.

12. C. L. Seitz, W.-K. Sun, "A family of routing and communication chips base mosaic", *Research on Integrated Systems*, *The M.I.T. Press*, Cambridge, MA,

13. K. van Berkel, R. Burgess, J. Kessels, M. Roncken, F. Schalij, A. Peeters, "Asynchronous circuits for low power: A DCC error corrector", *IEEE Design & T Comput.*, June 1994.
[Abstract] [PDF Full-Text (932KB)]

14. A. Yakovlev, A. I. Petrov, L. Lavagno, "A low latency asynchronous arbitra circuit", *IEEE Trans. VLSI Syst.*, vol.2, Sept. 1994.
[Abstract] [PDF Full-Text (584KB)]

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L9: Entry 1 of 12 File: USPT Sep 10, 2002

US-PAT-NO: 6449678
DOCUMENT-IDENTIFIER: US 6449678 B1

TITLE: Method and system for multiple read/write transactions across a bridge system

DATE-ISSUED: September 10, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Batchelor; Gary William	Tucson	AZ		
Ellison; Russell Lee	Corona De Tucson	AZ		
Jones; Carl Evan	Tucson	AZ		
Medlin; Robert Earl	Tucson	AZ		
Tafesse; Belayneh	Tucson	AZ		
Wade; Forrest Lee	Tucson	AZ		
Yanes; Juan Antonio	Tucson	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 275470 [PALM]
DATE FILED: March 24, 1999

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application is related to the following co-pending and commonly-assigned patent applications, which applications were filed on the same date herewith, and which applications are incorporated herein by reference in their entirety: "Method And System For Prefetching Data in a Bridge System," to Gary W. Batchelor, Carl E. Jones, Forrest Lee Wade, U.S. application Ser. No. 09/275,857; "Read Gather on Delayed Read Requests and Write Gather on Posted Write Operations for PCI Agents," to Gary W. Batchelor, Carl E. Jones, Dell P. Leabo, Robert E. Medlin, and Forrest Lee Wade, U.S. application Ser. No. 09/275,603; and "Delayed Read Continuation on Prefetched Data Non-Continuous Address," to Gary W. Batchelor, Brent C. Beardsley, Matthew J. Kalos, and Forrest Lee Wade, U.S. application Ser. No. 09/275,610.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/310; 710/306
US-CL-CURRENT: 710/310; 710/306

FIELD-OF-SEARCH: 710/129, 710/126, 710/127, 710/128, 710/7, 710/20, 710/52, 710/305, 710/306, 710/310, 710/311, 710/312, 710/313, 710/314, 710/315

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4490788	December 1984	Rasmussen	
☐	4947366	August 1990	Johnson	
☐	5404463	April 1995	McGarvey	
☐	5448704	September 1995	Spaniol et al.	
☐	5522050	May 1996	Amini et al.	
☐	5555383	September 1996	Elazar et al.	
☐	5574944	November 1996	Stager	
☐	5581714	December 1996	Amini et al.	
☐	5594878	January 1997	Shibata et al.	
☐	5603052	February 1997	Chejlava, Jr. et al.	
☐	5608884	March 1997	Potter	
☐	5632021	May 1997	Jennings et al.	
☐	5634033	May 1997	Stewart et al.	
☐	5644729	July 1997	Amini et al.	
☐	5649161	July 1997	Andrade et al.	
☐	5664117	September 1997	Shah et al.	
☐	5664124	September 1997	Katz et al.	
☐	5666551	September 1997	Fenwick et al.	
☐	5673399	September 1997	Guthrie et al.	
☐	5699529	December 1997	Powell et al.	
☐	5706469	January 1998	Kobayashi	
☐	5712986	January 1998	Vo	
☐	5721839	February 1998	Callison et al.	
☐	5721841	February 1998	Szczepanek	
☐	5724528	March 1998	Kulik et al.	
☐	5734841	March 1998	Shin et al.	
☐	5734847	March 1998	Garbus et al.	
☐	5737744	April 1998	Callison et al.	
☐	5740376	April 1998	Carson et al.	
☐	5740385	April 1998	Hayek et al.	
☐	5748920	May 1998	Mills et al.	
☐	5748921	May 1998	Lambrecht et al.	
☐	5758166	May 1998	Ajanovic	
☐	5761450	June 1998	Shah	
☐	5761462	June 1998	Neal et al.	

☐	5761725	June 1998	Zeller et al.	
☐	5764924	June 1998	Hong	
☐	5768548	June 1998	Young et al.	
☐	5835741	November 1998	Elkhoury et al.	710/129
☐	5991843	November 1999	Porterfield et al.	710/112
☐	6219737	April 2001	Chen et al.	710/129
☐	6256699	July 2001	Lee	710/126

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PCI Local Bus Specification; PCI Local Bus, Revision 2.1, Jun. 1, 1995 (Chapter 3.0, Appendix E).
PCI-to-PCI Bridge Architecture Specification, PCI Local Bus, Revision 1.1, Dec. 18, 1998 (Chapter 3, 4, 5).
PCI Local Bus Specification; PCI Local Bus, Revision 2.2, Dec. 18, 1998 (Chapter 1, 2, 3).
U.S. patent application Ser. No. 09/275,857 (TU9-98-072 18.42).
U.S. patent application Ser. No. 09/275,603 (TU9-98-073 18.43).
U.S. patent application Ser. No. 09/275,610 (TU9-98-074 18.44).

ART-UNIT: 2181

PRIMARY-EXAMINER: Wong; Peter

ASSISTANT-EXAMINER: Chung-Trans; X.

ABSTRACT:

Disclosed is a system for processing read/write transactions from a plurality of agents over a bus. The bridge includes at least one request buffer for each agent in communication with the bridge. The request buffer for an agent buffers transactions originating from that agent. The bridge further includes a return buffer for each agent in communication with the bridge. The return buffer for an agent buffers return data in connection with a transaction. Address translation circuitry is in communication with the bus and request and return buffers. The address translation circuitry locates a request buffer to queue the transaction, such that a transaction is stored in the request buffer corresponding to the agent that originated the transaction. Further, the address translation circuitry stores read return data for a read transaction in the return buffer corresponding to the agent originating the transaction.

30 Claims, 8 Drawing figures

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L9: Entry 6 of 12 File: USPT Mar 13, 2001

US-PAT-NO: 6202112
DOCUMENT-IDENTIFIER: US 6202112 B1

TITLE: Arbitration methods to avoid deadlock and livelock when performing transactions across a bridge

DATE-ISSUED: March 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gadagkar; Ashish	Sunnyvale	CA		
Bogin; Zohar	Folsom	CA		
Khandekar; Narendra	Folsom	CA		
Lent; David D.	Placerville	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 205351 [PALM]
DATE FILED: December 3, 1998

INT-CL: [07] G06 F 13/42

US-CL-ISSUED: 710/118; 710/112, 710/129
US-CL-CURRENT: 710/118; 710/112, 710/309

FIELD-OF-SEARCH: 710/105, 710/113-118, 710/112, 710/119-125, 710/241, 710/242, 710/129, 713/401

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4796022	January 1989	Schenkel et al.	
☐	4975829	December 1990	Clarey et al.	
☐	5278828	January 1994	Chao	
☐	5535340	July 1996	Bell et al.	710/112
☐	5611058	March 1997	Moore et al.	710/129
☐	5754802	May 1998	Okazawa et al.	710/129
☐	5949980	September 1999	Lee et al.	710/112
☐	5961623	October 1999	James et al.	710/113
☐	5974465	October 1999	Wong	709/234
☐	5999969	December 1999	Holmes et al.	709/213

ART-UNIT: 271

PRIMARY-EXAMINER: Myers; Paul R.

ABSTRACT:

An embodiment of the invention is directed at a bridge having an outbound pipe for buffering transaction information and data being transported from various devices to a bus. The bridge has an arbiter for granting requests associated with these devices to access the outbound pipe for transferring the transaction information and data into the pipe. The bridge generates a reject signal in response to an initial request associated with an initial transaction from a first one of the devices if the outbound pipe is unavailable to accept further transaction information or data. The bridge has response control logic for generating a retry response for the initial transaction in response to the reject signal. The bridge is able to assert a stamp signal in response to the reject signal. The arbiter in response to the stamp being asserted waits, without granting any other lower priority requests to access the outbound pipe, until a subsequent transaction from the first device makes progress.

33 Claims, 7 Drawing figures

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L9: Entry 7 of 12 File: USPT Feb 1, 2000

US-PAT-NO: 6021451
DOCUMENT-IDENTIFIER: US 6021451 A

TITLE: Method and apparatus for maintaining transaction ordering and arbitrating in a bus bridge

DATE-ISSUED: February 1, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bell; D. Michael	Beaverton	OR		
Gonzales; Mark A.	Portland	OR		
Meredith; Susan S.	Hillsboro	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 156175 [PALM]
DATE FILED: September 17, 1998

PARENT-CASE:
This is a continuation of application Ser. No. 08/889,756, filed Jul. 10, 1997, U.S. Pat. No. 5,835,739 which is a continuation of application Ser. No. 08/639,184, filed Apr. 26, 1996, abandoned, which is a continuation of application Ser. No. 08/246,776, filed May 20, 1994, now U.S. Pat. No. 5,546,546.

INT-CL: [06] G06 F 13/40

US-CL-ISSUED: 710/128; 710/100, 710/105, 710/112, 710/126, 710/129
US-CL-CURRENT: 710/309; 710/100, 710/105, 710/112, 710/310

FIELD-OF-SEARCH: 395/308, 395/292, 395/309, 395/306, 395/280, 395/285, 710/100, 710/112, 710/129, 710/126, 710/128, 710/105

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5191649	March 1993	Cadambi et al.	709/225
☐	5269005	December 1993	Heil et al.	710/49
☐	5307505	April 1994	Houlberg et al.	709/253
☐	5327570	July 1994	Foster et al.	712/30
☐	5333276	July 1994	Solari	712/220
☐	5369748	November 1994	Mcfarland et al.	710/126
☐	5546546	August 1996	Bell et al.	710/112
☐	5835739	November 1998	Bell et al.	710/128

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 524 684 A2	January 1993	EP	

OTHER PUBLICATIONS

Popescu, Val, et al., "The Metaflow Architecture," IEEE Micro, Jun. 1991, pp. 10-13 and 63-73.
Supplementary European Search Report dated Jul. 17, 1997 (2 pgs.).

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Jean; Frantz Blanchard

ABSTRACT:

A bus bridge situated between two buses includes two queues: an outbound request queue and an inbound request queue. Requests originating on the first bus which target a destination on the second bus are placed into the outbound request queue. Requests originating on the second bus which target a destination on the first bus are placed into the inbound request queue. A transaction arbitration unit (TAU) within the bridge maintains transaction ordering and avoids deadlocks. The TAU determines whether requests can be placed in the inbound request queue. The TAU also determines whether requests originating on the first bus can be responded to immediately or whether the agent originating the request must wait for a reply. In addition, the TAU includes logic for determining whether a request in the outbound request queue can be executed on the second bus. The TAU determines whether posting to the inbound request queue is enabled or disabled; whether any posted transactions exist in the inbound request queue; and whether ownership of the second bus is available.

32 Claims, 11 Drawing figures

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L9: Entry 8 of 12 File: USPT Nov 30, 1999

US-PAT-NO: 5996036
DOCUMENT-IDENTIFIER: US 5996036 A

TITLE: Bus transaction reordering in a computer system having unordered slaves

DATE-ISSUED: November 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Aptos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computers, Inc.	Cupertino	CA			02

APPL-NO: 08/ 779632 [PALM]
DATE FILED: January 7, 1997

INT-CL: [06] G06 F 9/46, G06 F 13/36, G11 C 7/00

US-CL-ISSUED: 710/110; 710/107, 709/208
US-CL-CURRENT: 710/110; 709/208, 710/107

FIELD-OF-SEARCH: 710/110, 710/107, 710/263, 710/41, 710/52, 711/151, 709/100-102, 709/208

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4181974	January 1980	Lemay et al.	364/900
☐	4473880	September 1984	Budde et al.	364/200
☐	4965716	October 1990	Sweeney	364/200
☐	5006982	April 1991	Ebersole et al.	710/263
☐	5191649	March 1993	Cadambi et al.	395/200
☐	5257356	October 1993	Brockmann et al.	395/725
☐	5287477	February 1994	Johnson et al.	395/425
☐	5327538	July 1994	Hamaguchi et al.	395/325
☐	5345562	September 1994	Chen	395/275
☐	5375215	December 1994	Hanawa et al.	395/425
☐	5473762	December 1995	Krein et al.	395/287
☐	5592631	January 1997	Kelly et al.	395/293
☐	5682512	October 1997	Tetrick	711/202
☐	5822772	October 1998	Chan et al.	711/158

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

17 Claims, 26 Drawing figures

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L9: Entry 9 of 12 File: USPT Aug 3, 1999

US-PAT-NO: 5933612
DOCUMENT-IDENTIFIER: US 5933612 A

TITLE: Deadlock avoidance in a split-bus computer system

DATE-ISSUED: August 3, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Aptos	CA		
Regal; Michael L.	Campbell	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 903412 [PALM]
DATE FILED: July 30, 1997

PARENT-CASE:
This application is a continuation of application Ser. No. 08/432,622, filed May 2, 1995 abandoned.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/306; 395/184.01, 395/200.54
US-CL-CURRENT: 710/311; 714/47

FIELD-OF-SEARCH: 395/184.01, 395/200.54, 395/726, 395/308, 395/306

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5442763	August 1995	Bartfai et al.	395/375
☐	5469435	November 1995	Krein et al.	370/85.2
☐	5473762	December 1995	Kelly et al.	395/287
☐	5542056	July 1996	Jaffa et al.	395/306
☐	5544332	August 1996	Chen	395/288
☐	5546546	August 1996	Bell et al.	395/292
☐	5592670	January 1997	Pletcher	395/670
☐	5680402	October 1997	Olnowich et al.	370/468

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Wiley; David A.

ABSTRACT:

A mechanism is provided for avoiding deadlock in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, transactions begun on said split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. The predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In accordance with another embodiment of the invention, the bus bridge detects when a state of the split-transaction bus would, if a protocol of said split-transaction bus were adhered to, result in deadlock. The bus bridge then drives one or more signals on the split-transaction bus in disregard of the protocol of the split-transaction bus, thereby avoiding deadlock. In accordance with still a further embodiment of the invention, transactions accepted within the bus bridge are monitored. When a combination of said transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. The predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock.

25 Claims, 18 Drawing figures

WEST

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L9: Entry 10 of 12 File: USPT Jul 27, 1999

US-PAT-NO: 5930485
DOCUMENT-IDENTIFIER: US 5930485 A

TITLE: Deadlock avoidance in a computer system having unordered slaves

DATE-ISSUED: July 27, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Aptos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 779913 [PALM]
DATE FILED: January 7, 1997

INT-CL: [06] G06 F 13/14, G06 F 13/40

US-CL-ISSUED: 395/292; 395/290, 395/293, 395/308
US-CL-CURRENT: 710/112; 710/110, 710/113, 710/309, 710/310

FIELD-OF-SEARCH: 395/290, 395/292, 395/293, 395/308, 395/309, 395/728, 395/729

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4494193	January 1985	Brahm et al.	364/200
☐	5305442	April 1994	Pedersen et al.	395/325
☐	5355455	October 1994	Hilgendorf et al.	395/325
☐	5363485	November 1994	Nguyen et al.	395/250
☐	5418914	May 1995	Heil et al.	395/325
☐	5442763	August 1995	Bartfai et al.	395/375
☐	5469435	November 1995	Krein et al.	370/85.2
☐	5473762	December 1995	Krein et al.	395/287
☐	5542056	July 1996	Jaffa et al.	395/306
☐	5544332	August 1996	Chen	395/288
☐	5546546	August 1996	Bell et al.	395/292
☐	5592631	January 1997	Kelly et al.	395/293
☐	5592670	January 1997	Pletcher	395/670
☐	5615343	March 1997	Sarangdhar et al.	395/282
☐	5680402	October 1997	Olnowich et al.	370/498
☐	5708794	January 1998	Parks et al.	395/481

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Pancholi; Jigar

ABSTRACT:

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on said split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

24 Claims, 28 Drawing figures

L5: Entry 11 of 14 File: USPT Jun 2, 1998

US-PAT-NO: 5761454
DOCUMENT-IDENTIFIER: US 5761454 A

TITLE: Deadlock resolution methods and apparatus for interfacing concurrent and asynchronous buses

DATE-ISSUED: June 2, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Adusumilli; Swaroop	Tempe	AZ		
Davis; Barry M.	Phoenix	AZ		
Fall; Brian N.	Chandler	AZ		
Richardson; Nicholas J.	La Jolla	CA		
Wszolek; Philip	Phoenix	AZ		

US-CL-CURRENT: 710/311; 710/105, 710/107, 710/108, 710/200, 710/36, 712/217

ABSTRACT:

A deadlock detection and resolution circuit for resolving a deadlock condition in a bridge circuit coupled to a memory, a host bus and a PCI bus of a computer system. The host bus and the PCI bus are configured to operate concurrently and asynchronously. The bridge circuit includes a host master circuit and a PCI slave circuit coupled between the host bus and the PCI bus and configured to service a PCI-MEMORY instruction from an external PCI master coupled to the PCI bus. A PCI master circuit and a host slave circuit within the bridge circuit couples between the PCI bus and the host bus and configured to service a CPU-PCI transaction from a CPU coupled to the host bus. The aforementioned deadlock condition occurs when the PCI-MEMORY transaction proceeds simultaneous with an issuance of the CPU-PCI transaction. The deadlock detection and resolution circuit includes first circuit for asserting an asynchronous handshake signal to the PCI slave of the bridge circuit. There is further included second circuit for determining whether the PCI slave is still able to complete the PCI-MEMORY transaction. Additionally, there is included third circuit for asserting an asynchronous handshake acknowledge signal to cancel the CPU-PCI transaction and removing the deadlock condition if the PCI slave is unable to complete the PCI-MEMORY transaction.

24 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

WEST

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Search Results - Record(s) 1 through 10 of 12 returned.

☐ 1. Document ID: US 6449678 B1

L9: Entry 1 of 12 File: USPT Sep 10, 2002

US-PAT-NO: 6449678
DOCUMENT-IDENTIFIER: US 6449678 B1

TITLE: Method and system for multiple read/write transactions across a bridge system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 2. Document ID: US 6425023 B1

L9: Entry 2 of 12 File: USPT Jul 23, 2002

US-PAT-NO: 6425023
DOCUMENT-IDENTIFIER: US 6425023 B1

TITLE: Method and system for gathering and buffering sequential data for a transaction comprising multiple data access requests

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 3. Document ID: US 6301632 B1

L9: Entry 3 of 12 File: USPT Oct 9, 2001

US-PAT-NO: 6301632
DOCUMENT-IDENTIFIER: US 6301632 B1

TITLE: Direct memory access system and method to bridge PCI bus protocols and hitachi SH4 protocols

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 4. Document ID: US 6286074 B1

L9: Entry 4 of 12 File: USPT Sep 4, 2001

US-PAT-NO: 6286074

DOCUMENT-IDENTIFIER: US 6286074 B1

TITLE: Method and system for reading prefetched data across a bridge system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 5. Document ID: US 6247102 B1

L9: Entry 5 of 12 File: USPT Jun 12, 2001

US-PAT-NO: 6247102
DOCUMENT-IDENTIFIER: US 6247102 B1

TITLE: Computer system employing memory controller and bridge interface permitting concurrent operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 6. Document ID: US 6202112 B1

L9: Entry 6 of 12 File: USPT Mar 13, 2001

US-PAT-NO: 6202112
DOCUMENT-IDENTIFIER: US 6202112 B1

TITLE: Arbitration methods to avoid deadlock and livelock when performing transactions across a bridge

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC
Draw. Desc | Image

☐ 7. Document ID: US 6021451 A

L9: Entry 7 of 12 File: USPT Feb 1, 2000

US-PAT-NO: 6021451
DOCUMENT-IDENTIFIER: US 6021451 A

TITLE: Method and apparatus for maintaining transaction ordering and arbitrating in a bus bridge

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw. Desc | Image

☐ 8. Document ID: US 5996036 A

L9: Entry 8 of 12 File: USPT Nov 30, 1999

US-PAT-NO: 5996036
DOCUMENT-IDENTIFIER: US 5996036 A

TITLE: Bus transaction reordering in a computer system having unordered slaves

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 9. Document ID: US 5933612 A

L9: Entry 9 of 12 File: USPT Aug 3, 1999

US-PAT-NO: 5933612
DOCUMENT-IDENTIFIER: US 5933612 A

TITLE: Deadlock avoidance in a split-bus computer system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 10. Document ID: US 5930485 A

L9: Entry 10 of 12 File: USPT Jul 27, 1999

US-PAT-NO: 5930485
DOCUMENT-IDENTIFIER: US 5930485 A

TITLE: Deadlock avoidance in a computer system having unordered slaves

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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Terms	Documents
l3 and L7	12

Display Format: TI Change Format

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Search Results - Record(s) 11 through 12 of 12 returned.

☐ 11. Document ID: US 5835739 A

L9: Entry 11 of 12 File: USPT Nov 10, 1998

US-PAT-NO: 5835739
DOCUMENT-IDENTIFIER: US 5835739 A

TITLE: Method and apparatus for maintaining transaction ordering and arbitrating in a bus bridge

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

☐ 12. Document ID: US 5546546 A

L9: Entry 12 of 12 File: USPT Aug 13, 1996

US-PAT-NO: 5546546
DOCUMENT-IDENTIFIER: US 5546546 A

TITLE: Method and apparatus for maintaining transaction ordering and arbitrating in a bus bridge

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Image

Generate Collection | Print

Terms	Documents
l3 and L7	12

Display Format: TI Change Format

Previous Page Next Page

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 5996036 A

L1: Entry 1 of 2 File: USPT Nov 30, 1999

US-PAT-NO: 5996036
DOCUMENT-IDENTIFIER: US 5996036 A

TITLE: Bus transaction reordering in a computer system having unordered slaves

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5933612 A

L1: Entry 2 of 2 File: USPT Aug 3, 1999

US-PAT-NO: 5933612
DOCUMENT-IDENTIFIER: US 5933612 A

TITLE: Deadlock avoidance in a split-bus computer system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

Generate Collection | Print

Terms	Documents
5933612.pn. or 5996036.pn.	2

Display Format: TI Change Format

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WEST

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L1: Entry 1 of 2 File: USPT Nov 30, 1999

US-PAT-NO: 5996036
DOCUMENT-IDENTIFIER: US 5996036 A

TITLE: Bus transaction reordering in a computer system having unordered slaves

DATE-ISSUED: November 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Aptos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computers, Inc.	Cupertino	CA			02

APPL-NO: 08/ 779632 [PALM]
DATE FILED: January 7, 1997

INT-CL: [06] G06 F 9/46, G06 F 13/36, G11 C 7/00

US-CL-ISSUED: 710/110; 710/107, 709/208
US-CL-CURRENT: 710/110; 709/208, 710/107

FIELD-OF-SEARCH: 710/110, 710/107, 710/263, 710/41, 710/52, 711/151, 709/100-102, 709/208

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4181974	January 1980	Lemay et al.	364/900
☐	4473880	September 1984	Budde et al.	364/200
☐	4965716	October 1990	Sweeney	364/200
☐	5006982	April 1991	Ebersole et al.	710/263
☐	5191649	March 1993	Cadambi et al.	395/200
☐	5257356	October 1993	Brockmann et al.	395/725
☐	5287477	February 1994	Johnson et al.	395/425
☐	5327538	July 1994	Hamaguchi et al.	395/325
☐	5345562	September 1994	Chen	395/275
☐	5375215	December 1994	Hanawa et al.	395/425
☐	5473762	December 1995	Krein et al.	395/287
☐	5592631	January 1997	Kelly et al.	395/293
☐	5682512	October 1997	Tetrick	711/202
☐	5822772	October 1998	Chan et al.	711/158

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

17 Claims, 26 Drawing figures

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L1: Entry 2 of 2 File: USPT Aug 3, 1999

US-PAT-NO: 5933612
DOCUMENT-IDENTIFIER: US 5933612 A

TITLE: Deadlock avoidance in a split-bus computer system

DATE-ISSUED: August 3, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelly; James D.	Aptos	CA		
Regal; Michael L.	Campbell	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 903412 [PALM]
DATE FILED: July 30, 1997

PARENT-CASE:
This application is a continuation of application Ser. No. 08/432,622, filed May 2, 1995 abandoned.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/306; 395/184.01, 395/200.54
US-CL-CURRENT: 710/311; 714/47

FIELD-OF-SEARCH: 395/184.01, 395/200.54, 395/726, 395/308, 395/306

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5442763	August 1995	Bartfai et al.	395/375
☐	5469435	November 1995	Krein et al.	370/85.2
☐	5473762	December 1995	Kelly et al.	395/287
☐	5542056	July 1996	Jaffa et al.	395/306
☐	5544332	August 1996	Chen	395/288
☐	5546546	August 1996	Bell et al.	395/292
☐	5592670	January 1997	Pletcher	395/670
☐	5680402	October 1997	Olnowich et al.	370/468

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Wiley; David A.

ABSTRACT:

A mechanism is provided for avoiding deadlock in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, transactions begun on said split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. The predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In accordance with another embodiment of the invention, the bus bridge detects when a state of the split-transaction bus would, if a protocol of said split-transaction bus were adhered to, result in deadlock. The bus bridge then drives one or more signals on the split-transaction bus in disregard of the protocol of the split-transaction bus, thereby avoiding deadlock. In accordance with still a further embodiment of the invention, transactions accepted within the bus bridge are monitored. When a combination of said transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. The predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock.

25 Claims, 18 Drawing figures